Umeå University
Department of Computing Science
5DV008 — Computer Architecture
Examination: January 14, 2011

Name (printed): _____

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Instructions: / Instruktioner:

This examination will be graded anonymously. This page will be removed before the instructor receives the examination for grading. The secret code number given above must therefore be written on every answer page which you turn in to the examination proctor.

Denna skrivning rättas kodad. Detta blad kommer att avskiljas innan läraren får skrivningen för rättning. Ovanstående kod måste därför finnas på samtliga svarsblad när du lämnar skrivningen till skrivvakten.

To the proctor of the examination: / Till skrivningsbevakaren:

Detach this cover sheet from the examination and put it in the envelope which is addressed to Yvonne Löwstedt, Department of Computing Science.

Avskilj detta försättsblad och stoppa i kuvert som skickas till Yvonne Löwstedt, Datavetenskap.

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1. Answers may be written in English or Swedish. However, all technical terms which do not have an absolutely standard representation in Swedish must be given in English.

2. A pocket engineering calculator (miniräknare) and English/X - X/English dictionary may be used. No other help materials are allowed.

3. Answers must be written on the official university answer sheets which are provided the sheets in numerical order of the problems, and write on only one side of the paper. Write only the question number and your secret code number on these pages; do not write your name or ID.

4. Show your work. For questions which require that an answer be computed, numerical answers without derivations will not receive credit. It is furthermore a good idea to show the symbolic formula used to obtain the answer, since that will result in more credit in the case that an error is made.

5. The examination has a total of 1000 points.

6. For problems with multiple parts, you have the choice, for each part, to do the problem, or to skip it for partial credit. In the table below, place an X in the position for any problem for which you have attempted a solution, and which you wish to have graded. It is extremely important that you fill in this table properly, because of the following option. For any box which is left blank, the associated question will not be graded, and you will instead be awarded 15% of the points for that question. Your decision to leave a box blank is definitive, so be very careful. For example, If you leave box 8(b) blank, your answer to that question will not be graded, even if it is completely correct. On the other hand, if you place an X in box 8(b), but provide no answer whatsoever to that question, you will not receive 15% of the points for that question. It is strongly recommended that you use a pencil, in case you change your mind!

Prob	1	2	3	4	5	6	7	8
(a)								
(b)	■							
(c)	■						■	

(1: 100 points total) An issue known as the *power wall* has had a profound impact upon the nature of microprocessors which have been developed in recent years. Explain what the power wall is and how the design of recent microprocessors has changed to address the problems which it imposes.

(2: 125 points total) Consider a MIPS load instruction of the following form, where n is some number.

$$\text{lw \$t1, (n)\$t2}$$

(a: 25 points) Identify the range of numerical values which are allowed for n.

(b: 50 points) Illustrate how this instruction is represented, field by field, as a 32-bit word in MIPS. It is not necessary to give the opcode or numerical values for the register names, but all other information should be provided.

(c: 50 points) Explain precisely how the memory address whose contents is to be loaded is computed.

(3: 100 points total) Consider a floating-point number represented using IEEE 754 format:

$$(-1)^{\text{Sign}} \times \text{Significand} \times 2^{\text{Exponent}}$$

(a: 40 points) In *normalized* format, the value of the significand satisfies $n_1 \leq \text{Significand} < n_2$. Give the values for n_1 and n_2.

(b: 45 points) The Significand is usually represented in a compact form as a *fraction*. Explain what this means and illustrate with a simple example. Identify in particular how much storage is saved via this representation.

(c: 40 points) The exponent is usually represented in *bias* format. Explain what this means and why this representation is preferable to two's complement.

(4: 125 points total) An implementation of the MIPS architecture following the model developed in the textbook has the following delays for each of the five main stages:

Component	Delay
Instruction fetch (IF)	150 ps.
Instruction decode and register file read (ID)	100 ps.
Execution or address calculation (EX)	250 ps.
Data memory access (MEM)	125 ps.
Write back (WB)	70 ps.

(a: 50 points) Assuming a non-pipelined implementation, and assuming all delays not explicitly identified above to be negligible, compute the latency for each of the five instructions `addi`, `bne`, `jr`, `lw`, and `sw`.

(b: 50 points) Repeat part (a), this time assuming a pipelined implementation with the five stages identified above.

(c: 25 points) Suppose that the instruction mix of a program is as follows: `add`: 10%; `mul`: 10%; `beq`: 30%; `jr`; 10%; `lw`: 15%; `sw`: 25%. For the pipelined implementation, compute the percentage of total cycles which utilize data memory. Assume that there are no stalls or hazards.

(5: 150 points total) Given is the following instruction sequence.

```
lw   $t1, 0($t2)
sub  $t3, $t2, $t1
sw   $t4, 0($t3)
add  $t3, $t1, $t1
sub  $t1, $t1, $t2
sra  $t3, $t2, 12
xor  $t5, $t1, $t2
```

(a: 50 points) Identify all *read after write* (RAW) data dependencies, regardless of the distance. (Note: These dependencies are called *read before write* in the slides.)

(b: 50 points) For the five-stage pipeline model of the textbook, indicate which of these dependencies results in a hazard in the case that there is no forwarding, and show how `nop` operations may be inserted to avoid these hazards. Find one solution for the instruction sequence which resolves all hazards, not one solution for each hazard. The solution must not contain any unnecessary `nop`'s.

(c: 50 points) Repeat part (b) in the case that forwarding is employed. Insert `nops` only in the case that the hazard cannot be avoided by forwarding alone.

(6: 125 points total) A two-way set-associative cache is to hold 128K bytes of data. Assuming that a one-bit valid field is required (for each way), answer the following questions for one-word data blocks (per way), for words of 32 bits.

(a: 40 points) Determine the size of the tag field (for each way).

(b: 40 points) Compute the size of the index needed for the cache.

(c: 45 points) Compute the total number of bits required for the cache.

Hint: Draw a picture of a typical row in this cache, to make sure that you have accounted for all things. (A row consists of all of the elements for a given index — n elements for an n-way set-associative cache.) The total size is then the size of one row times the number of rows. If you draw such a row correctly, it will help the grader understand what you did, and may result in greater partial credit in case there are errors in your solution.

(7: 150 points total) Consider a processor with an L1 cache for the MIPS instruction set and the following parameters.

Ideal CPI	5
Miss rate for access to instruction memory	1%
Miss penalty for access to instruction memory	100 clock cycles
Miss rate for access to data memory	2%
Miss penalty for access to data memory	100 clock cycles
Instruction mix	Load 10%, Store 15%, Arithmetic 65%, Branch 10%

(a: 75 points) Compute the actual CPI for this processor-cache pair.

(b: 75 points) Repeat (a), this time assuming that there is also a unified L2 cache with with a miss penalty of 20 clock cycles and a miss rate of 0.10%.

(8: 125 points total) Give general answers to the following. Your answers need not be detailed (since these topics were not covered in detail in the course), but they should contain enough information to show that you understand the fundamental ideas.

(a: 45 points) Give the equation underlying *Amdahl's Law* and explain clearly what each of its parameters denotes..

(b: 40 points) Two fundamental forms of multiprocessor interconnection and communication are *SMP* and *MPP*. Explain how memory is organized in each of these, how the processors communicate with each other, and describe very briefly the advantages and disadvantages of each.

(c: 40 points) A predominant configuration for multiprocessor systems today is the *cluster*. Describe briefly what is meant by a cluster and explain the advantages which have made them so popular.