

Umeå University
Department of Computing Science
5DV008 — Computer Architecture
Examination: January 13, 2010

Name (printed): _____

Swedish ID number: _____

Computer User-ID: _____

Signature: _____

Secret code number: _____

Instructions: / Instruktioner:

This examination will be graded anonymously. This page will be removed before the instructor receives the examination for grading. The secret code number given above must therefore be written on every answer page which you turn in to the examination proctor.

Denna skrivning rättas kodad. Detta blad kommer att avskiljas innan läraren får skrivningen för rättning. Ovanstående kod måste därför finnas på samtliga svarsblad när du lämnar skrivningen till skrivvakten.

To the proctor of the examination: / Till skrivningsbevakaren:

Detach this cover sheet from the examination and put it in the envelope which is addressed to Yvonne Löwstedt, Department of Computing Science.

Avskilj detta försättsblad och stoppa i kuvert som skickas till Yvonne Löwstedt, Datavetenskap.

Umeå University
Department of Computing Science
5DV008 — Computer Architecture
Examination: January 13, 2010

Secret code number: _____

1. Answers may be written in English or Swedish. However, all technical terms which do not have an absolutely standard representation in Swedish must be given in English.
2. A pocket engineering calculator (miniräknare) and English/X - X/English dictionary may be used. No other help materials are allowed.
3. Answers must be written on the official university answer sheets which are provided the sheets in numerical order of the problems, and write on only one side of the paper. Write only the question number and your secret code number on these pages; do not write your name or ID.
4. Show your work. For questions which require that an answer be computed, numerical answers without derivations will not receive credit. It is furthermore a good idea to show the symbolic formula used to obtain the answer, since that will result in more credit in the case that an error is made.
5. The examination has a total of 1000 points.
6. For problems with multiple parts, you have the choice, for each part, to do the problem, or to skip it for partial credit. In the table below, place an X in the position for any problem for which you have attempted a solution, and which you wish to have graded. It is extremely important that you fill in this table properly, because of the following option. For any box which is left blank, the associated question will not be graded, and you will instead be awarded 15% of the points for that question. Your decision to leave a box blank is definitive, so be very careful. For example, If you leave box 8(b) blank, your answer to that question will not be graded, even if it is completely correct. On the other hand, if you place an X in box 8(b), but provide no answer whatsoever to that question, you will not receive 15% of the points for that question. It is strongly recommended that you use a pencil, in case you change your mind!

Prob	1	2	3	4	5	6	7	8
(a)								
(b)			■					
(c)			■					■

(1: 125 points total) In the MIPS instruction set, there are three distinct types of instructions which can alter the value of the PC (program counter). Answer the following questions regarding these.

(a: 50 points) Consider an instruction of the following form: `beq $t1, $t2, Label`

Clarify how the actual 32-bit address corresponding to `Label` is computed as a combination of a value stored within the instruction and the value of the PC (program counter). Your answer must include in particular the size in bits of the value which is stored in the instruction, as well as how it is modified and then combined with the PC to determine the full 32-bit instruction. Also, identify the range of addresses which may be represented in this fashion.

(b: 50 points) Repeat part (a) for an instruction of the following form: `j Label`

(c: 25 points) Consider an instruction of the following form: `jr $t1`

Clarify how the actual 32-bit address for the next instruction is determined in this case. Also, identify the range of addresses which may be represented in this fashion.

(2: 100 points total) Answer the following questions about the representation of floating-point numbers using IEEE 754 format.

(a: 50 points) A certain computer with a 32-bit word size uses a floating-point representation in which there is one sign bit, a 10-bit exponent field, and a 21-bit fraction field. Give the range of normalized values which can be represented in this format. You need not and should not consider denormalized values. This range should be expressed in terms of simple combinations of powers of two.

(b: 25 points) The exponent is represented in *bias* format. Explain what this means and why this representation is preferable to two's complement.

(c: 25 points) Explain how *NaN* (not a number) is represented in this format.

(3: 100 points total) A laptop-computer hard drive has the parameters given in the table below. Compute the average amount of time required to read or write one 512-byte sector.

Parameter	Value
Rotational speed	4200 rpm
Seek time	15 ms.
Controller overhead	1 ms.
Transfer rate	25M bytes/sec.

(4: 125 points total) An implementation of the MIPS architecture following the model developed in the textbook has the following delays for each of the five main stages:

Component	Delay
Instruction fetch (IF)	100 ps.
Instruction decode and register file read (ID)	75 ps.
Execution or address calculation (EX)	250 ps.
Data memory access (MEM)	125 ps.
Write back (WB)	50 ps.

- (a: 50 points) Assuming a non-pipelined implementation, and assuming all delays not explicitly identified above to be negligible, compute the latency for each of the five instructions `add`, `beq`, `j`, `lw`, and `sw`.
- (b: 50 points) Repeat part (a), this time assuming a pipelined implementation with the five stages identified above.
- (c: 25 points) Suppose that the instruction mix of a program is as follows: `add`: 10%; `mul`: 10%; `beq`: 30%; `jr`: 10%; `lw`: 15%; `sw`: 25%. For the pipelined implementation, compute the percentage of total cycles which utilize data memory. Assume that there are no stalls or hazards.

(5: 150 points total) Given is the following instruction sequence.

```

addi $t2, $t3, 50
sub  $t3, $t1, $t2
sra  $t4, $t2, 12
xor  $t5, $t1, $t2
sw   $t1, 0($t2)
lw   $t3, 0($t2)
sw   $t3, 0($t1)

```

- (a: 50 points) Identify all *read after write* (RAW) data dependencies, regardless of the distance. (Note: These dependencies are called *read before write* in the slides.)
- (b: 50 points) For the five-stage pipeline model of the textbook, indicate which of these dependencies results in a hazard in the case that there is no forwarding, and show how `nop` operations may be inserted to avoid these hazards. Find one solution for the instruction sequence which resolves all hazards, not one solution for each hazard. The solution must not contain any unnecessary `nop`'s.
- (c: 50 points) Repeat part (b) in the case that forwarding is employed.

(6: 125 points total) Answer the following questions concerning address spaces and their support within computer hardware.

- (a: 45 points) Explain the difference between a *physical address* and a *virtual address*.
- (b: 40 points) Explain what a *translation lookaside buffer (TLB)* is, and clarify its rôle in the support of efficient cache processing.
- (c: 40 points) The address associated with a cache entry is typically a physical address and not a virtual address. Clarify the reason for this design decision.

(7: 125 points total) A direct-mapped cache is to hold 64K bytes of data. Assuming that a one-bit valid field is required, answer the following questions for two-word data blocks. (A word is 32 bits.)

- (a: 40 points) Determine the size of the tag field.
- (b: 40 points) Compute the total number of bytes required for the cache.
- (c: 45 points) Compute the size of the index needed for the cache.

(8: 150 points total) Consider a processor with an L1 cache for the MIPS instruction set and the following parameters.

Ideal CPI	5
Miss rate for access to instruction memory	2%
Miss penalty for access to instruction memory	70 clock cycles
Miss rate for access to data memory	3%
Miss penalty for access to data memory	80 clock cycles
Instruction mix	Load 10%, Store 20%, Arithmetic 50%, Branch 20%

- (a: 75 points) Compute the actual CPI for this processor-cache pair.
- (b: 75 points) Repeat (a), this time assuming that there is also a unified L2 cache with with a miss penalty of 25 clock cycles and a miss rate of 0.30%.