5DV118 **Computer Architecture** **Fall 2012**

Problem Exercise 2

Due date: January 7, 2013 at 1640 (4:40pm)

This is the second of two problem exercises. It is not obligatory, but it does carry points which may be used to offset a weaker score on the examination, as described in the course syllabus. This exercise is worth at total of 50 points. The due date is strict and late submissions will not be accepted, except under extenuating circumstances.

Problems similar to these may appear on examinations. It is therefore advisable to know how to solve such problems.

1 Problems

1. A direct-mapped cache is to hold 32 KBytes of data. Assuming that a one-bit valid field is required, answer the following questions for (a) one-word data blocks, and (b) four-word data blocks. (A word is 32 bits.)

(i) Determine the size of the tag field.

(ii) Compute the total number of bits required for the cache.

(iii) Compute the size of the index field needed for the cache.

2. A direct-mapped cache consists of eight blocks of four 32-bit words each. The sequence of byte addresses shown in the table below indicates the references which are made to the cache. Assuming that the cache is initially empty, for each such address, indicate the following by making the appropriate entry in the table.

(i) The index (also known as line id, block id) of the block in the table.

(ii) The letter `H` or `M`, depending upon whether the reference results in a hit or a miss to the cache.

(iii) The letter `N` or `Y`, depending upon whether or not the current block must be replaced. Making an initial entry into a block which does not hold a valid entry is not considered a replacement.

Byte Address	32	16	24	76	88	104	164	224	168	244	148	64	192
Index													
Hit/Miss													
Replace													

3. Consider a processor with an L1 cache for the MIPS instruction set and the following parameters.

Ideal CPI	3
Miss rate for access to instruction memory	2%
Miss penalty for access to instruction memory	75 clock cycles
Miss rate for access to data memory	7%
Miss penalty for access to data memory	100 clock cycles
Instruction mix	Load 20%, Store 10%, Arithmetic 60%, Branch 10%

(a) Compute the actual CPI for this processor-cache pair.

(b) Repeat (a), this time assuming that there is also a unified L2 cache with a miss penalty of 20 clock cycles and a miss rate of 0.2%.

4. A memory system operates on a bus which is one-word (32-bits) wide. It is governed by the following parameters:

Time to send the address to memory	1 clock cycle
Row cycle time	25 clock cycles
Column access time	10 clock cycles
Time to return one word from memory	2 clock cycles

(a) Compute the number of clock cycles necessary to fetch one word from memory.

(b) Compute the number of clock cycles necessary to fetch eight words from memory, assuming that the memory is not interleaved, and that there are two blocks of four words, with the words of each block in the same row, but the two blocks in different rows.

(c) Compute the number of clock cycles necessary to fetch eight words from memory, assuming that the memory is interleaved, and that each word of a four-block word is in a different bank of the memory. Assume further that the two blocks are in different rows.

2 Submission Rules

Solutions may be developed and submitted by groups of up to three individuals.

A printed copy of the solution must be placed in the appropriate course mailbox on the fourth floor of MIT-huset. The user-id of each group member for the submission must be indicated clearly on a cover page of the printed submission.

Students who will be away from Umeå on January 7 may **by prior arrangement** submit solutions electronically. These arrangements must be made **well in advance** with the grader.